What Is Claimed Is:

1. An LSI design method including a formation of wiring patterns in an interconnection wiring layer, the method comprising:

a layout process for forming a wiring pattern in the interconnection wiring layer from logic data including a plurality of cells and connections thereof;

a dummy pattern generation process for inserting conductive dummy patterns continuous in the direction perpendicular to said wiring patterns between said wiring patterns, which are adjacent and extend in the same direction, at a first distance from said adjacent wiring patterns; and

a capacitance extraction process for extracting a value of capacitance between said adjacent wiring patterns where said dummy pattern is generated as a capacitance value corresponding to said first distance.

2. The LSI design method according to claim 1, wherein said dummy pattern generation process comprises a process for generating a dummy pattern over the entire area in said interconnection wiring layer and then removing the dummy pattern present in the region within the first distance from the wiring patterns.

3. The LSI design method according to claim 1, wherein a characteristic of capacitance between said adjacent wiring patterns includes a first region where the value of capacitance between the adjacent wiring patterns greatly changes in response to changes in a distance of a dielectric region between the adjacent wiring patterns and a second region where the value of capacitance changes are less than in the first region, and in said dummy pattern generation process, said first distance is selected as a value corresponding to a minimum distance in said second region.

4. The LSI design method according to claim 1, wherein a characteristic of capacitance between said adjacent wiring patterns includes a first region where the value of capacitance between the adjacent wiring patterns greatly changes in response to changes in a distance of a dielectric region between the adjacent wiring patterns and a second region where the value of capacitance changes are less than in the first region, and in said dummy pattern generation process, the first distance is selected as a value corresponding to a predetermined distance in said first region.

5. The LSI design method according to claim 1, wherein a characteristic of capacitance between said

adjacent wiring patterns includes a first region where the value of capacitance between the adjacent wiring patterns greatly changes in response to changes in a distance of a dielectric region between the adjacent wiring patterns and a second region where the value of capacitance changes are less than in the first region; and

wherein, in said dummy pattern generation process, the first distance is selected as a value corresponding to a minimum distance in said second region and a predetermined distance in said first region; and

in said capacitance extraction process, when a distance between said wiring patterns and dummy patterns is selected as a value corresponding to said minimum distance, a first capacitance value corresponding to said minimum distance is extracted, and when the distance between said wiring patterns and dummy patterns is selected as a value corresponding to said predetermined distance, a second capacitance value corresponding to said predetermined distance is extracted.

6. The LSI design method according to claim 4 or 5, wherein, in said dummy pattern generation process, the generation of dummy pattern is not conducted when a distance between said adjacent wiring patterns is

not more than the doubled said predetermined distance; and

wherein, in said capacitance extraction process, the capacitance value corresponding to the distance between the adjacent wiring patterns is extracted for the wiring patterns for which no dummy pattern was generated.

7. The LSI design method according to claim 1, wherein in said dummy pattern generation process, the generation of dummy pattern is not conducted when a distance between said adjacent wiring patterns is not more than the doubled said first distance, and in said capacitance extraction process, the capacitance value corresponding to the distance between the adjacent wiring patterns is extracted for the wiring patterns for which no dummy pattern was generated.

8. An LSI design computer program for executing in a computer an LSI design process including a formation of wiring patterns in an interconnection wiring layer, the LSI design process comprising:

a layout process for forming a wiring pattern in the interconnection wiring layer from logic data including a plurality of cells and connections thereof;

a dummy pattern generation process for inserting

conductive dummy patterns continuous in the direction perpendicular to said wiring patterns between said wiring patterns, which are adjacent and extend in the same direction, at a first distance from said adjacent wiring patterns; and

a capacitance extraction process for extracting a value of capacitance between said adjacent wiring patterns where said dummy pattern is generated as a capacitance value corresponding to said first distance.

9. The LSI design computer program according to claim 8, wherein said dummy pattern generation process comprises a process for generating a dummy pattern over the entire area in said interconnection wiring layer and then removing the dummy pattern present in the region within the first distance from the wiring patterns.

10. The LSI design computer program according to claim 9, wherein a characteristic of capacitance between said adjacent wiring patterns includes a first region where the value of capacitance between the adjacent wiring patterns greatly changes in response to changes in a distance of a dielectric region between the adjacent wiring patterns and a second region where the value of capacitance changes are less than in the first region, and in said dummy pattern

generation process, said first distance is selected as a value corresponding to a minimum distance in said second region.

11. The LSI design computer program according to claim 9, wherein a characteristic of capacitance between said adjacent wiring patterns includes a first region where the value of capacitance between the adjacent wiring patterns greatly changes in response to changes in a distance of a dielectric region between the adjacent wiring patterns and a second region where the value of capacitance changes are less than in the first region, and in said dummy pattern generation process, the first distance is selected as a value corresponding to a predetermined distance in said first region.

12. The LSI design computer program according to claim 9, wherein a characteristic of capacitance between said adjacent wiring patterns includes a first region where the value of capacitance between the adjacent wiring patterns greatly changes in response to changes in a distance of a dielectric region between the adjacent wiring patterns and a second region where the value of capacitance changes are less than in the first region; and

wherein, in said dummy pattern generation process,

said first distance is selected as a value corresponding to a minimum distance in said second region and a predetermined distance in said first region; and

in said capacitance extraction process, when a distance between said wiring patterns and dummy patterns is selected as a value corresponding to said minimum distance, a first capacitance value corresponding to said minimum distance is extracted, and when the distance between said wiring patterns and dummy patterns is selected as a value corresponding to said predetermined distance, a second capacitance value corresponding to said predetermined distance is extracted.

13. A semiconductor device comprising:

a plurality of wiring patterns formed in an interconnection wiring layer; and

conductive dummy patterns inserted continuously in a direction perpendicular to said wiring patterns between said wiring patterns, which are adjacent and extend in the same direction, at a first distance from said adjacent wiring patterns.

14. The semiconductor device according to claim 13, wherein a characteristic of capacitance between said adjacent wiring patterns includes a first region

where the value of capacitance between the adjacent wiring patterns greatly changes in response to changes in a distance of a dielectric region between the adjacent wiring patterns and a second region where the value of capacitance changes are less than in the first region, and said first distance corresponds to a minimum distance in said second region.

15. The semiconductor device according to claim 13, wherein a characteristic of capacitance between said adjacent wiring patterns includes a first region where the value of capacitance between the adjacent wiring patterns greatly changes in response to changes in a distance of a dielectric region between the adjacent wiring patterns and a second region where the value of capacitance changes are less than in the first region, and said first distance corresponds to a predetermined distance in said first region.

16. The semiconductor device according to claim 13, wherein a characteristic of capacitance between said adjacent wiring patterns includes a first region where the value of capacitance between the adjacent wiring patterns greatly changes in response to changes in a distance of a dielectric region between the adjacent wiring patterns and a second region where the value of capacitance changes are less than in the

first region, wherein said plurality of conductive dummy patterns includes first conductive dummy patterns for which said first distance corresponds to a minimum distance in said second region, and second conductive dummy patterns for said first distance corresponds to a predetermined distance in said first region.